REMARKS

The enclosed is responsive to the Office Action mailed on January 23, 2006. At the time the Office Action was mailed claims 1-14, 16, 26, 27, and 29-41 were pending.

The Applicant thanks the Examiner for indicating allowing claims 10-14 and 16.

By way of the present response Applicants have: 1) amended claims 1, 26, 30, and 35; 2) added no new claims; and 3) canceled no new claims. As such, claims 1-14, 16, 26, 27, and 29-41 remain pending. The Applicant respectfully request reconsideration of the present application and allowance of all claims now presented

Amendments to Claims 1, 26, and 30

The Applicant notes that, unintentionally, the amendment to the preamble of claim 1, the preamble of claim 26, and the last limitation of claim 30, submitted in the response filed on November 19, 2004, was not propagated to subsequent responses listing the claims. The amendments to the preamble to claim 1, the preamble of claim 26, and the last limitation of claim 30, submitted herein, correlates to the amendments previously filed on November 19, 2004. The Applicant apologizes for any confusion.

35 U.S.C. § 102 Rejections

The Office rejected claims 1-8, 26, 27, 31-34, and 36-41 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,570,221 by Allman (hereinafter, "*Allman*"). The Applicant respectfully traverses.

Claims 1, 26, and 39 are each independent claims.

Claim 1 includes the limitation of "forming a layer of second material between the two substrates of the stacked device, wherein the second material causes a reaction in a portion of the first material." *Allman* does not disclose or suggest this limitation.

Allman describes "the use of spin-on-glass (SOG) to bond two layers of semiconductor together, in order to form a Silicon-on-Insulator (SOI) structure. One type of SOG is a cross-linked siloxane polymer, preferably of the poly-organo-siloxane type..." (*Allman*, Abstract).

The Office Action cites col. 4, lines 36-52 and FIG. 8C of *Allman* as disclosing the limitation of claim 1 of: "forming a layer of second material between the two substrates of the

stacked device, wherein the second material causes a reaction in a portion of the first material," asserting that the two substrates are the first and second device wafers of *Allman* and that the reaction is cross-linking. (Office Action, 1/23/06, p. 3).

Col. 4, lines 36-52 of *Allman* states:

> Some embodiments could form a multi-layered IC where two wafers are joined using SOG such that transistors from one wafer face transistors from another wafer. In one embodiment, **a highly cross-linked siloxane polymer bonds the two wafers together using the SOG technique discussed above**. With reference to FIG. 8A, a first device wafer includes a first transistor layer with various circuits deposited thereon in a conventional manner. In FIG. 8B, a second device wafer is shown that includes a second transistor layer with various circuit deposited thereon in the conventional manner. **A SOG layer is applied to the second device wafer in a manner similar to that discussed in relation to FIG. 3B above**. After the first and second device wafers are joined, a multi-layer device is produced as shown in FIG. 8C. Those skilled in the art can appreciate that the method described above in relation to FIGS. 3A and 3B can be used to join the first and second device wafers. (*Allman*, col. 4, lines 36-52 (emphasis added)).

In *Allman*, the "techniques discussed above" and "in relation to FIG. 3B" describe applying SOG on a wafer, placing another wafer in contact with the SOG, and curing the SOG to bond the two wafers together. *Allman* describes:

> ...**spin-on-glass (SOG) is applied** to the SUBSTRATE WAFER, as indicated. SOG is known in the art....The SOG is applied to a thickness ranging from 1,000 to 30,000 Angstroms. (To achieve thicknesses in the higher levels of this range, **repeated SOG coatings may be necessary, using a baking step** at a temperature exceeding 80 degrees C. between coatings **to remove solvents and to initiate cross-linking**.) Next, **another silicon wafer (a DEVICE WAFER) is placed in contact with the SOG**, as shown in FIG. 3B. The **SOG is then cured** at a temperature between 300 C. and 1400 C..... **The cured SOG forms a siloxane polymer**, which bonds the two wafers together." (*Allman*, col. 2, lines 25-45, emphasis added).

In *Allman*, the curing ("at a temperature between 300 C. and 1400 C. in either (a) vacuum, (b) room air, (c) nitrogen, (d) forming gas, (e) argon, (f) HMDS, (g) oxygen, or (h) a mixture of these gases") initiates cross-linking in the SOG. (See *Allman*, col. 2, lines 41-44).

Allman does not describe a layer of second material formed between the two substrates that causes a reaction in the SOG ("the first material"). Accordingly, *Allman* does not disclose or suggest "forming a layer of second material between the two substrates of the stacked device, wherein the second material causes a reaction in a portion of the first material," as required by claim 1. Therefore, *Allman* does not anticipate claim 1.

Claim 26 includes the limitation of "reacting a portion of the layer of material, wherein the reaction results in the portion of the layer of material increasing in volume." *Allman* also does not disclose or suggest this limitation.

The Office Action cites col. 4, lines 36-52 and FIG. 8C of *Allman* as disclosing this limitation. (Office Action, 1/23/06, p. 4). Specifically, the Office Action appears to assert that cross-linking results in the portion of the SOG increasing in volume." (*See*, Office Action, 1/23/06, p. 4).

The cited section indicates that "a highly cross-linked siloxane polymer bonds the two wafers together using the SOG technique discussed above." (*Allman*, col. 4, lines 39-41). The SOG technique of *Allman* is described as "curing the SOG" and as maybe including "a baking step at a temperature exceeding 80 degrees C. between coatings to remove solvents and to initiate cross-linking." (*Allman*, col. 2, lines 36-45). Baking to removing solvents generally reduces volume, not increases volume.

Additionally, FIGS. 8B-8C of *Allman* (reproduced below) does not disclose or suggest any increase in the volume of the layer of SOG material:

FIG. 8C

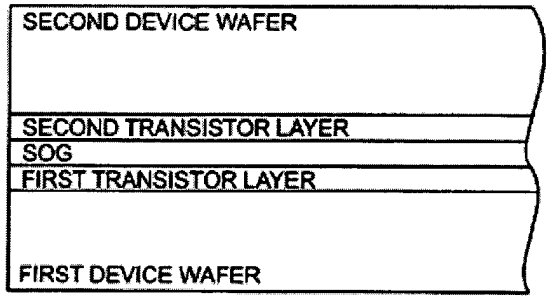
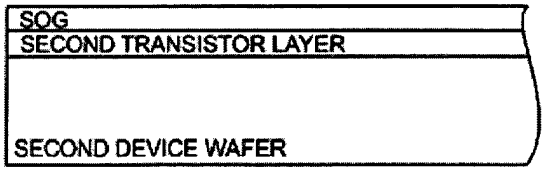


FIG. 8B



Accordingly, *Allman* does not disclose or suggest "reacting a portion of the layer of material, wherein the reaction results in the portion of the layer of material increasing in volume," as required by claim 26. Therefore, *Allman* does not anticipate claim 26.

Claim 39 includes the limitation of "providing a foam filling an area between the first and second wafers adjacent to the first and second conductive interconnect structures." *Allman* also does not disclose or suggest this limitation.

As discussed above, *Allman* describes applying SOG on a wafer, placing another wafer in contact with the SOG, and curing the SOG to bond the two wafers together. The "cured SOG forms a siloxane polymer, which bonds the two wafers together." (*Allman*, col. 2, lines 44-45). *Allman* describes the "SOG is preferably a layer of cross-linked siloxane polymer sandwiched between the wafers." (*Allman*, col. 5, lines 8-9). Accordingly, in *Allman*, a siloxane polymer is formed on a wafer, another wafer is placed in contact with the siloxane polymer, and the siloxane polymer is cured to bond to the two wafers.

As the Examiner correctly stated with regard to claims 9, 29, 30, and 35, "*Allman* does not explicitly disclose that the reaction produces a polymer foam." (Office Action, 1/23/06, p. 8). *Allman* does not explicitly disclose foam. *Allman* does not disclose or suggest that the curing of the siloxane polymer provides a foam filling an area between the first and second wafer. Accordingly, *Allman* does not disclose or suggest "providing a foam filling an area between the first and second wafers adjacent to the first and second conductive interconnect structures," as required by claim 39. Therefore, *Allman* does not anticipate claim 39.

Claims 2-8, 27, and 40-41 depend, directly or indirectly from one of the foregoing independent claims 1, 26 or 39. Accordingly, *Allman* does not anticipate claims 2-8, 27, and 40-41 for at least the foregoing reasons.

Claims 31-34 and 36-38 depend, directly or indirectly, from independent claims 30 and 35, respectively. As correctly stated by the Examiner, "In re claims...30, 35 *Allman* does not explicitly disclose that the reaction produces a polymer foam." (Office Action, 1/23/06, p. 8). Accordingly, *Allman* does not anticipate the independent claims 30 and 35. Therefore, *Allman* cannot anticipate claims 31-34 and 36-38 which depend, directly or indirectly, from independent claims 30 and 35, respectively.

Accordingly, the Applicant respectfully requests withdrawal of the rejections to claims 1-8, 26, 27, 31-34, and 36-41 under 35 U.S.C. § 102(e) as being anticipated by *Allman*.

35 U.S.C. § 103 Rejections

The Office Action has rejected claims 9, 29, 30, and 35 under 35 U.S.C. § 103(a) as being unpatentable over *Allman* in view of U.S. Patent 6,168,737 by Poco et al. (hereinafter, "*Poco*"). The Applicant respectfully traverses.

Claim 9 and claim 29 depend from independent claims 1 and 26, respectively. The Applicant submits that, because claim 9 and claim 29 depend from patentable independent claims, claim 9 and 29 are also patentable.

Moreover, regarding claim 9, which depends from claim 1, *Allman* does not disclose or suggest the limitation of claim 1, as discussed above, of "forming a layer of second material between the two substrates of the stacked device, wherein the second material causes a reaction in a portion of the first material."

The Applicant submits that *Poco* also does not disclose or suggest this limitation, as discussed in the previous response (mailed on November 3, 2005) with regard to a rejection to claim 1 under 35 U.S.C. § 102 over *Poco*, which rejection was withdrawn in response to the Applicant's response. (*See* Office Action, 1/23/06, p. 2). Accordingly, claim 1 is patentable over *Allman* and *Poco*. Accordingly, the Applicant submits that claim 9, which depends from claim 1, is also patentable over *Allman* and *Poco*.

Furthermore, regarding claim 29, which depends from claim 26, *Allman* does not disclose or suggest the limitation of claim 26, as discussed above, of "reacting a portion of the layer of material, wherein the reaction results in the portion of the layer of material increasing in volume."

The Applicant submits that *Poco* also does not disclose or suggest this limitation, as discussed in the previous response (mailed on November 3, 2005) with regard to a rejection to claim 26 under 35 U.S.C. § 102 over *Poco*, which rejection was withdrawn in response to the Applicant's response. (*See* Office Action, 1/23/06, p. 2). Accordingly, claim 26 is patentable over *Allman* and *Poco*. Accordingly, the Applicant submits that claim 29, which depends from claim 26, is also patentable over *Allman* and *Poco*.

Claim 30, as amended, recites the limitation of "filling a portion of an area between the two substrates with a polymer foam as a product of a reaction between the first material and the second material."

As the Examiner correctly stated, "*Allman* does not explicitly disclose that the reaction produces a polymer foam." (Office Action, 1/23/06, p. 8). Accordingly, Allman does not disclose or suggest the limitation of "filling a portion of an area between the two substrates with a polymer foam as a product of a reaction between the first material and the second material."

Poco also does not disclose or suggest this limitation. *Poco* describes: "The term "porous dielectric material" as used here includes microporous and mesoporous solids having open and connected pores, such as polymer foams, pre-ceramics, porous glasses, aerogels, and xerogels. The porous material is formed from a precursor solution that is dried by removing the liquid from a two-phase liquid-solid network." (*Poco*, col. 3, lines 27-33, emphasis added). Accordingly, in *Poco*, the polymer foam is a product of drying a precursor solution.

Poco does not disclose or suggest that the polymer foam is a product of a reaction between a first material and a second material. Accordingly, *Poco* also does not disclose or suggest the limitation missing from *Allman* of "filling a portion of an area between the two substrates with a polymer foam as a product of a reaction between the first material and the second material." Therefore, claim 30 is patentable over *Allman* and *Poco*.

Claim 35 recites the limitation of "removing a portion of the layer of material such that a top surface of the layer of material is lower than a top surface of the interconnect structure to expose the top surface of the interconnect structure." Neither *Allman*, nor *Poco*, individually or in combination, disclose or suggest this limitation.

The Office Action cites the "metal interconnect pillar" of *Allman* as the interconnect structure of claim 35. (Office Action, 1/23/06, p. 8). Metal interconnect pillars are shown in FIG. 6 of *Allman*. *Allman* does not use the term "metal," "interconnect," or "pillar" in the specification. *Allman* describes:

> A representative cross-section is shown in FIG. 6. Then, SOG is applied, as described above, and a second DEVICE WAFER is applied, as shown, and polished, to reduce its thickness. The SOG is cured, and additional ICs are manufactured on the second DEVICE WAFER. Vias are fabricated, as known in the art, connecting selected points on

the first DEVICE WAFER with those on the second. (*Allman*, col. 4, lines 19-27, emphasis added).

Accordingly, in *Allman*, the "metal interconnect pillars" shown in FIG 6. correspond to the "vias" described in the specification of *Allman*. *Allman* describes:

> The fabrication procedure for the second layer of ICs will involve heating steps which will probably alter the doping profiles of the first layer.... To avoid this alteration, it may be desirable to fabricate the first and second DEVICE WAFERs separately. These layers are *then* attached using the SOG procedure. Connecting vias are fabricated, as known in the art. (*Allman*, col. 4, lines 28-35, emphasis added).

Allman claims "15. The multi-layer integrated circuit according to claim 10, further comprising vias which couple the micro-machined sensor to the transistor, wherein the vias penetrate the layer of highly cross-linked siloxane polymer." (Allman, claim 15, emphasis added).

Allman does not explicitly disclose or suggest the method by which the "metal interconnect pillars" (or vias) in *Allman* are formed. The language in *Allman* suggests, however, that the "metal interconnect pillars" (or vias) are formed to penetrate through the SOG layer after the SOG layer is formed. Even if the bottom pillar was formed prior to the formation of the SOG layer, and the top via was formed to penetrate the SOG layer and connect to the bottom pillar, there is no disclosure or suggestion in *Allman* of removing a portion of the SOG layer such that a top surface of the SOG layer is lower than a top surface of the metal interconnect pillar.

Accordingly, *Allman* does not disclose or suggest the limitation of "removing a portion of the layer of material such that a top surface of the layer of material is lower than a top surface of the interconnect structure to expose the top surface of the interconnect structure," as required by claim 35.

Poco also does not disclose or suggest this limitation. As discussed in the previous response (mailed on November 3, 2005) with regard to a rejection to claim 35 under 35 U.S.C. § 102 over *Poco*, which rejection was withdrawn in response to the Applicant's response (*see* Office Action, 1/23/06, p. 2), *Poco* does not disclose or suggest an interconnect structure. Therefore, *Poco* does not disclose or suggest the limitation of: "removing a portion of the layer of material such that a top surface of the layer of material is lower than a top surface of the interconnect structure to expose the top surface of the interconnect structure."

Accordingly, claim 35 is patentable over *Allman* and *Poco*.

Accordingly, the Applicant respectfully requests withdrawal of the rejection to claims 9, 29, 30, and 35 under 35 U.S.C. § 103(a) as being unpatentable over *Allman* in view *Poco*.

CONCLUSION

The Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Ms. Van N. Nguy or Mr. Michael A. Bernadicou at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Van N. Nguy
Reg. No. 55,851

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300